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Temperature-dependent electrical characteristics analysis of the Al/*p*-type Si structures with GO and PTCDA interlayer: structural properties

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ABSTRACT

In this study, the electrical characteristics of ***Al*/*p-type Si*** semiconductor structures with PTCDA and GO interlayer were analyzed using current–voltage (*I-V*) measurements a wide temperature range (from 80 to 420 K with 20 K intervals and ± 2.0 V). The ideality factor (n) and barrier height (Φ_{bo}) values changed between 6.398 and 1.330 and 0.221 eV and 0.999 eV (**for thermionic emission, *TE*, method),** 0.243 eV and 1.084 eV (for Norde method) in temperature range of 80 K and 420 K, respectively. The experimental findings revealed that values of ideality factors (n), rectification ratio (***RR***) and series resistance (R_S) decreases with increasing temperature, while barrier heights (Φ_{bo}) and saturation currents (I_0) values increases with increasing temperature. The Φ_{bo}–n and Φ_{bo}-$q/(2kT)$ curves were obtained to explain the high n values and non-ideal situations of the Richardson curves. Two linear regions were found at low temperatures (from 80 to 180 K) and high temperatures (from 200 to 420 K). Thus, for low and high temperatures, Gaussian distributions (***GDs***) values of the $I-V$ plot of the ***Al*/(*PTCDA:GO*)/*p*-type Si** semiconductor structure yielded average barrier heights of 0.7017 and 1.3342 eV with standard deviations (σ_0) of 83.06 mV and 168.80 mV, respectively. Also, this values of barrier height have also been confirmed by updated $ln(I_0/T^2) - (q^2\sigma_s^2)/(2k^2T^2)$ vs. $q/(kT)$ curves, which correspond to two distinct temperature regions. Richardson constant (A^*) value with 1.153×10^{-6} $A/(K^2cm^2)$ is lower than the known value of ***p*-type Si**. But nevertheless, for distribution 1, Richardson's constant of 80.64 $A/(K^2cm^2)$ is approximately three times larger than the known theoretical value of 32 $Acm^{-2}\,K^{-2}$ for ***p*-type** silicon.

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1 Introduction

Metal–semiconductor interface semiconductor structures are devices that play an important role in electronic circuits and have certain advantages over metal–semiconductor structures. The most commonly used rectifier contacts in the electronics industry include metal-semiconductors (***MS***), metal-oxide-semiconductors (***MOS***), and metal–insulator-semiconductor (***MIS***) structures [1–12]. Silicon (***Si***) semiconductor is a semiconductor material that is the fourth group in the periodic table. Due to the oxide layer on the ***Si*** surface, ***Si*** semiconductor structure is broadly used in electrical and/or electronic circuit components. Therefore, ***Si***-based semiconductor structures are used in the electronics industry and are considered as the indispensable basic component of integrated circuits and microchip circuits. Graphene oxide (***GO***) thin films have been widely researched in the last years because of superior applications in electronic industries. **Thus, it is also widely used in electrical and electronic circuit components owing to the thin graphene oxide (*GO*) layer on the silicon (*Si*) surface. Oxygen-containing graphene oxide (*GO*) is used not only for the interlayer in the electronics industry but also for optoelectronic and microelectronic applications' thermal stability. Due to their successful properties, *GO*-interfaced MS structures are used in wide diversity of technical applications such as solar cells applications, supercapacitors, light-emitting diodes, biosensors, photodetectors and field-effect transistors. This demonstrates the effective use of graphene oxide-based materials in electrical circuit components** [13–20]**. At the same time, *GO* can also be used to create nano-composite semiconductor structures instead of high purity graphene.** In short, since graphene oxide, which is essentially a single molecule layer of high graphite, is very important material, "Andre Geim and Kostya Novoselov were awarded the Nobel Prize in 2004" for research on graphene [21, 22].

PTCDA, also known as perylene tetracarboxylic dianhydride, is an organic semiconductor and dye molecule, and PTCDA is used in many research areas, including energy storage technologies [23–25]**. *PTCDA* thin films provide very good conductive transport properties due to their high crystallinity and low intermolecular distance in the crystal** [26–32]. **Thus, *PTCDA*, an organic dye molecule, provides excellent electrochemical performance and electrical conductivity when used at the *MS* interface. Because of this features, field-effect transistors and organic photovoltaic devices also heavily depend on *PTCDA* organic dye molecules.** There are very few studies in the literature regarding ***PTCDA*** organic dye molecules used in the MS interface. For example, Berk and et al. [32] have been studied electrical properties of Al/***GO:PTCDA***/*p*-type Si photodiode semiconductor structures at room temperature. Soylu and et al. [33] examined electrical properties of the Ag/ ***PTCDA***/*p*-type GaAs structure and observed that it exhibited rectifying behavior. Karataş [4] studied the different electrical properties of *Al*/***p*-type** Si and *Al*/***PTCDA***/*p*-type Si semiconductor structures at room temperature (300 K) and their role on the interfacial state densities. But in this study, a thin semiconductor organic layer of ***GO:PTCDA*** prepared in equal amounts was deposited on the ***Si*** substrate by spin coating method. Because of its many benefits, including low temperature processing, low cost, and simple mass manufacturing, spin coating technology was employed. Examining electrical characteristics and conduction mechanisms of semiconductor structures at 300 K does not provide us with comprehensive device information. Thus, in order to comprehensive understanding of the electrical properties of the ***Al***/***GO:PTCDA***/p-type Si structures, we examined an analysis of the *I-V* characteristics in a wide temperature ranges (from 80 to 420 K by steps 20 K), and we can learn the basic characteristics of the ***Al***/***GO:PTCDA***/*p*-type ***Si*** structures as detail over wide temperature ranges. Few investigations have been done on the temperature-dependent electrical characteristics of ***Al***/***GO:PTCDA***/***p-Si*** structures, despite the fact that several studies on the temperature-dependent electrical properties of ***Al***/***p-type Si MS*** structures have been published in the literature. Also, as mentioned above, it is impossible to fully understand the properties of semiconductor structures only at room temperature. Because the ideality factors, the series resistances of semiconductor diodes in forward bias state and the potential barrier created at the ***MS*** interface provide us with important information about the electronic properties of these devices [34–39]. Therefore, our study's primary goal is to construct an ***Al***/***(GO:PTCDA)***/***p-type-Si*** semiconductor structure with ***GO:PTCDA*** interface layers and investigate the semiconductor structure's electrical and conduction characteristics throughout a temperature range of 80–420 K. Electrical properties of ***Al***/***GO:PTCDA***/***p-type Si*** semiconductor structures according to the thermionic emission (***TE***)

method were investigated using ***I-V*** measurements. The n, Φ_{bo}, I_0, RR, and R_S values were determined independently for each temperature. Because of the barrier heights (***BHs***) inhomogeneity that exists at ***MOS*** interfaces, temperature-dependent BHs of ***Al/GO:PTCDA/p-type Si*** semiconductor structures were interpreted based on existence of ***GDs*** of ***BHs*** around a mean value.

2 Methods and materials

For this investigation, we bought ***PTCDA*** and ***GO*** organic semiconductor powder from Fytronix, however we used Sigma-Aldrich chemical solvents to clean the substrates. The ***Si*** crystal that was utilized to produce the semiconductor structure has a resistance structure of 2–10 Ω-cm and a thickness of 525 μm in the [100] direction. In order to clear impurities from the semiconductor surfaces, the wafer was first cleaned using the RCA1 cleaning procedure [1, 9, 10, 40, and 41]. The wafer was dried using nitrogen gas (N_2) after the cleaning procedure. After, Al (99.999 percent) metal was evaporated at $\mathbf{10^{-6}}$ Torr for ohmic contact using a thermal evaporation equipment. The wafer was annealed using a dry nitrogen gas flow at 500 °C for three minutes. The Si wafer was then divided into tiny pieces. Under the same circumstances, **Al/PTCDA:GO (1:1)/*p*-type Si** structures were prepared for the small wafer substrates. ***PTCDA:GO*** thin organic layer solution was prepared in chloroform as a 1:1 solution (10^{-3} mol L^{-1}). Using the spin coating method (6800 Spin Coater Series), ***PTCDA:GO*** (1:1) solutions were coated to the front faces of semiconductor wafers for 30 s at a spin speed of 1000 rpm. After these processes, ***Al*** metal was thermally evaporated onto the surface of the organic layer semiconductor pieces at a pressure of 10^6 Torr to form an Al (99.999% purity) metal contact with a diameter of 1 mm (rectifier contact area = 7.85×10^{-3} cm^2). Additionally, more information about production techniques has been provided in your previous works [12, 14, 40, and 41]. **The cross section of the Al/PTCDA:GO/*p*-type Si semiconductor structure is as shown in** Fig. 1 **(a). Temperature-dependent *I-V* measurements of the prepared Al/PTCDA:GO/*p*-type Si semiconductor structure were taken using electronic devices as seen in** Fig. 1 **(b). Additionally, the energy band diagram of the *Al/PTCDA:GO/p-type Si* structure is as shown in** Fig. 1(c)**. If we define the terms in the expressions in** Fig. 1 **(c), Φ_m is work function of the metal, Φ_s is work function of the semiconductor, χ_s is electron affinity of the semiconductor, δ is thickness of the *GO:PTCDA* interface layer, E_F is the Fermi energy, E_V is valence band of the semiconductor and E_C is conduction band of the semiconductor.** All measurements were performed with the help of an IEEE-488 AC/DC converter board and a computer.

3 Results and discussion

Scanning Electron Microscope (Zeiss EVO 10LS-SEM) was used to analyze the structural properties of **GO** and ***PTCDA*** powder. The solid state UV-V spectra of **GO** and ***PTCDA*** organic semiconductor powders are shown in Figs. 2 (a) and 2 (b), respectively. Thus, with the same way, Figs. 2 (c) and (d) show surface morphologies of **GO:PTCDA** organic powders, respectively. Since sufficient information is given about UV and SEM pictures of ***GO*** and PTCDA structures in references 31 and 32, there is no need to give it again here. Therefore, detailed information about UV and SEM pictures of ***GO*** and ***PTCDA*** organic structures is given in refs. 31 and 32, respectively.

Figure 3 shows the temperature-dependent *I–V* measurements of the ***Al/(PTCDA:GO)/p-type Si*** structures. As seen in Fig. 3, the ***Al/PTCDA:GO/p-type Si*** semiconductor structure shows very good rectification properties. Thus, the basic electrical values such as Φ_{bo}, n, I_0, RR, and R_S of the Al/GO:PTCDA/p-type Si semiconductor structure were obtained from the ***I–V*** characteristics. As shown from Fig. 3, although current values increase rapidly depending on temperature at low voltages, current values remain constant at high voltages due to the effect of series resistance. The fact of matter is that the current starts to bend in the high voltages owing to the effect of series resistance. Thus, according to thermionic emission model, relationship between current (I) and voltage (V) is written as follows [1, 2, 4, 9–14, 31–34, 37–44];

$$I = AA^{*}T^{2}\exp\left(\frac{-q\Phi_b}{kT}\right)\left[\exp(\frac{q(V-IR_S)}{nkT}-1)\right] \quad (1)$$

where, the meaning of the abbreviation in Eq. 1 is as follows;

q is elementary charge (1.602×10^{-19} C),
I_0 is saturation current,

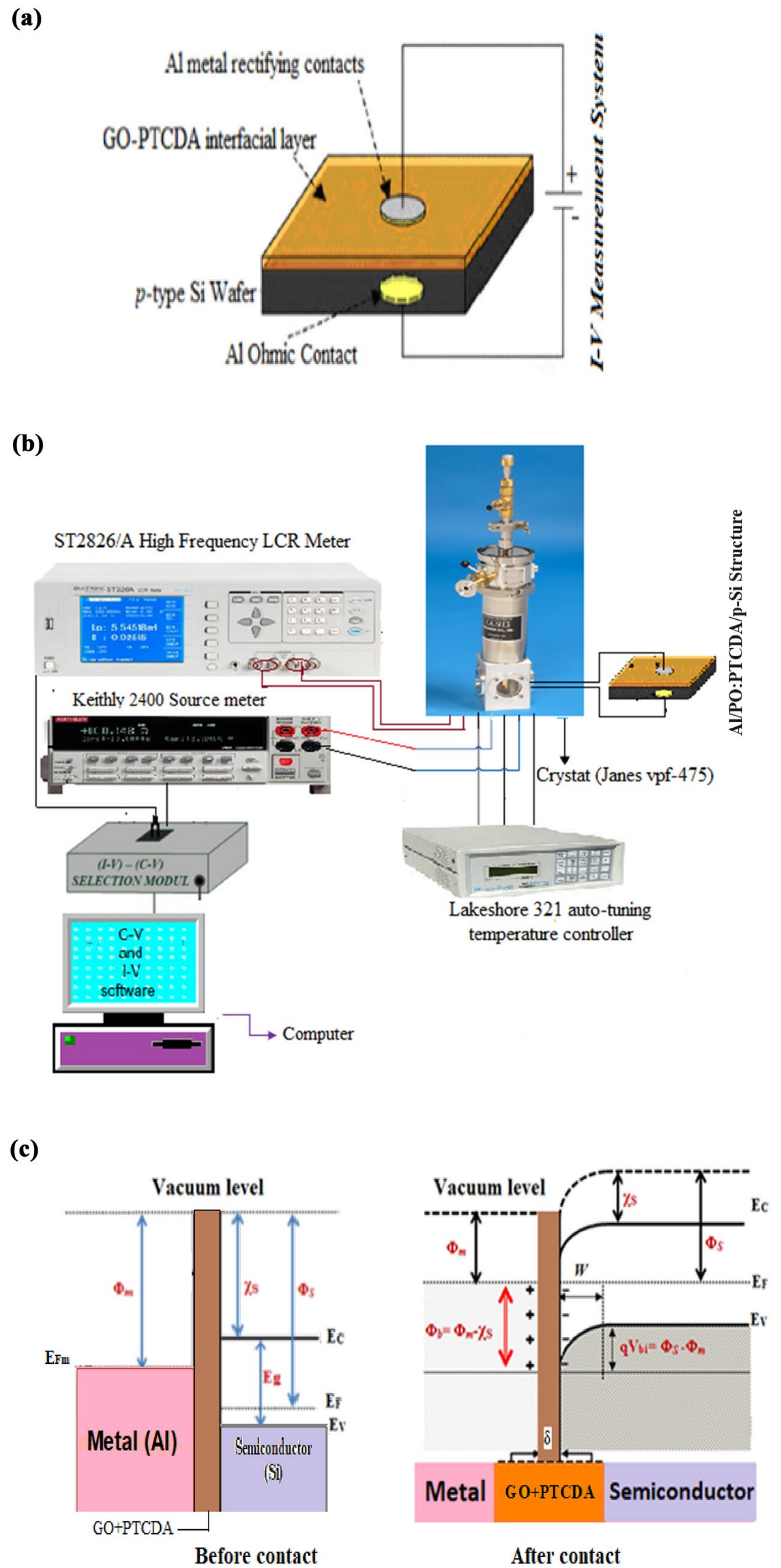

Fig. 1 For the Al/GO:PTCDA/p-type Si structure; **a** Schematic cross-section, **b** the detailed scheme of I-V measurement system, and (**c**) Before contact and after contact energy band diagram [31], respectively

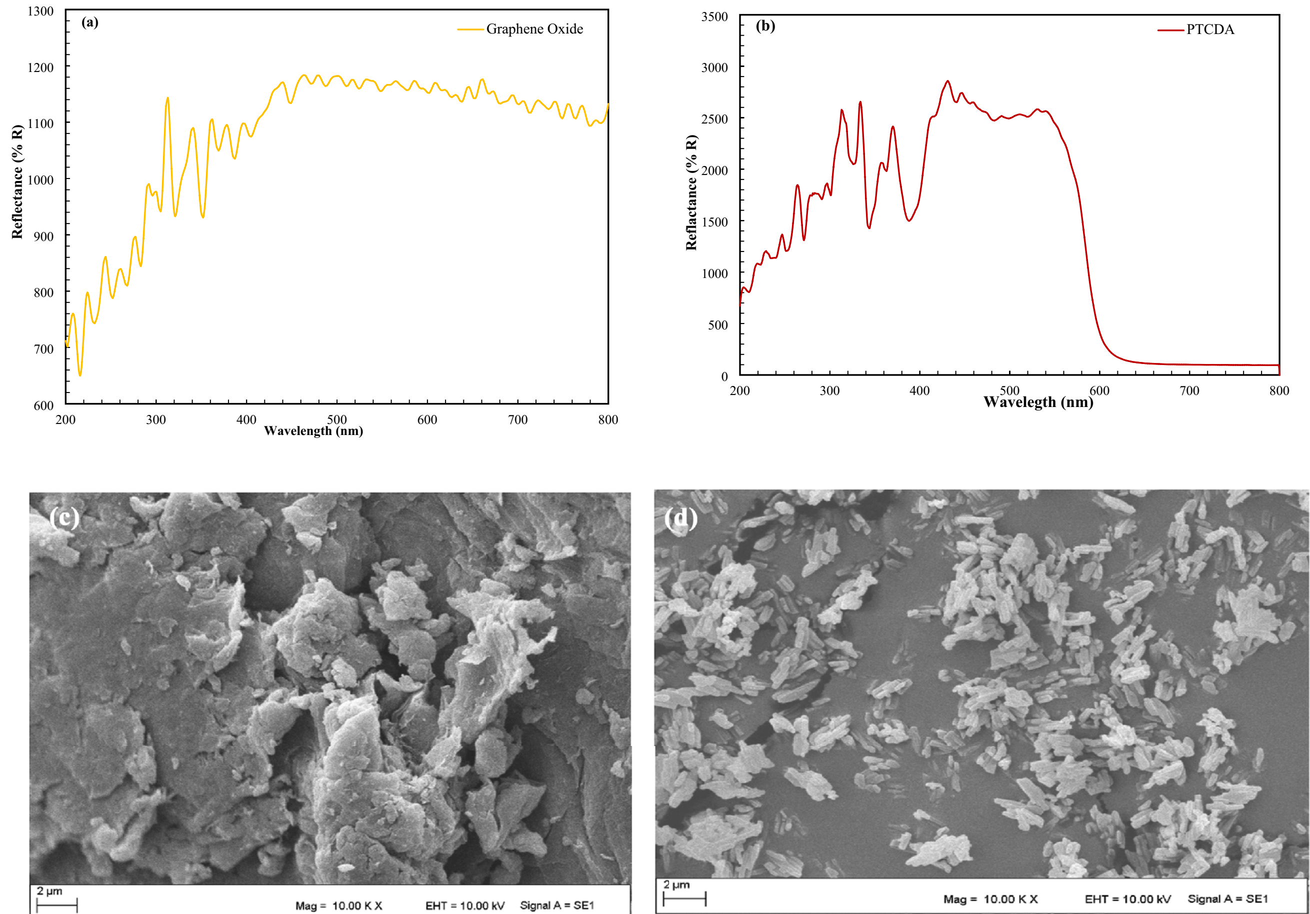

Fig. 2 **a** UV/Vis spectrum of GO, **b** UV/Vis spectrum of PTCDA, **c** SEM image of GO and **b** SEM image of PTCDA, respectively

I is current value,
V is applied voltage
R_S is series resistance,
T is **absolute** room temperature (**for 300 K**), respectively.
k is Boltzmann constant (1.38×10^{-23} J/K), and
n is ideality factor,

here, the I_0 and *n* values can be calculated from the fit lines of the linear part of the ln*I*-*V* plots. From Eq. 1, the I_0 can written as follows [1, 2, 9–14, 31–35, and 38–45];

$$I_O = AA^*T^2 \exp\left(-\frac{q\Phi_{bo}}{kT}\right) \tag{2}$$

from Eq. 2;

A is area of the rectifying contact of ***Al/(GO:PTCDA)/p-type Si*** semiconductor diode (7.85×10^{-3} cm^2),
A^* is Richardson value for *p*-type Si (32 Acm^{-2} K^{-2}) [1, 9],
Φ_{bo} is barrier heights of the ***Al/(GO:PTCDA)/p-type Si*** structure, respectively.

If both equality is 1 and equality 2 are rearranged, the values of *n* and Φ_b can be calculated from the following equations;

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \tag{3}$$

and

$$\Phi_{bo} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_O}\right) \tag{4}$$

The values *of the n* and Φ_{bo} for each temperatures were calculated form Eqs. (3, 4), respectively. The obtained *n* and Φ_b values are shown in Fig. 4 and this values are also shown Table 1. As seen in Fig. 4 and

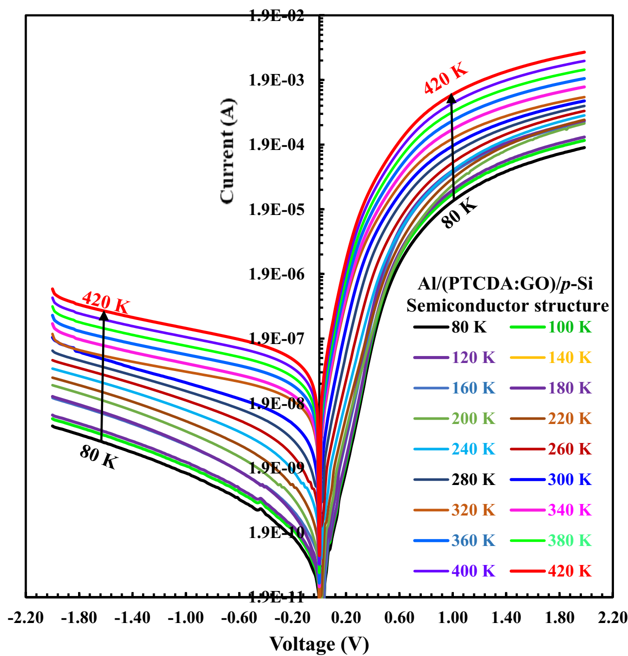

Fig. 3 The lnI–V curves of the Al/GO:PTCDA/p-Si structure in the temperature ranges of 80–420 K

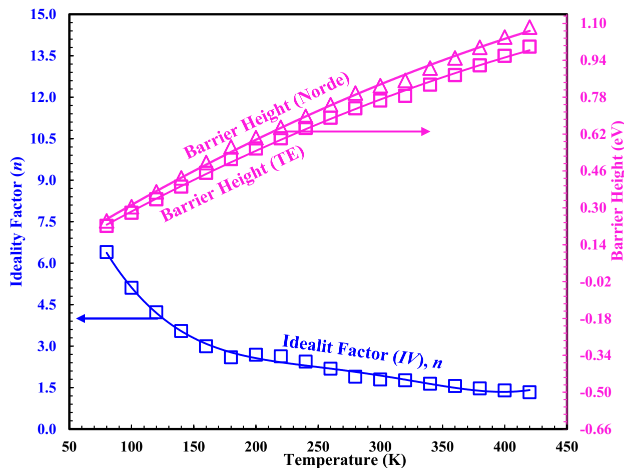

Fig. 4 Change of barrier heights and ideality factors of Al/GO:PTCDA/p-Si structure as a function of temperature

Table 1, the values of n increase from 1.330 at 420 K to 6.398 at 80 K, whereas the barrier heights (Φ_b for *TE*) values decrease from 0.999 at 420 K to 0.221 eV at 80 K. Thus, according to ***TE*** theory, the n value for semiconductor structure is one. But, values of the ideality factors we obtained in this study are greater than 1. Therefore, we can say that the decrease in the idealite factor as the temperature increases for the ***Al/GO:PTCDA/p-type S***i semiconductor structures indicates deviations from thermionic emission (***TE***) theory. This can be attributed to the MS interface state and therefore to barrier inhomogeneity at interface. At the same time, shown in Table 1, saturation current values increased by increasing temperature for ***Al/GO:PTCDA/p-type S***i semiconductor structure [45–49]. Also, very high values of ideality factors can be attributed to the presence of thin oxide layer at interface. This means that we can say that the ***Al/GO:PTCDA/p-type S***i device can recommended for temperature-dependent situations in technology. Furthermore, especially for low temperatures, low barrier height values correspond to larger ideality values, and this indicates inhomogeneity of barrier height at interface. This means that at low temperature charge carriers don't have enough energy to overcome high barriers. In other words, since the kinetic energy of carriers is weak at low temperatures, they can pass through low barriers, and therefore the barrier height is expected to increase due to increasing temperature. Another parameter that shows whether semiconductor structures are good circuit elements is the rectifier ratio (***RR***). The ratio of forward current to reverse current at a particular voltage is called the ***RR*** value of a semiconductor structure. Therefore, the *RR* equation is written as follows;

$$RR = IF/IR \tag{5}$$

here; IF is the current values at + 1.0 V or + 2.0 V in forward regions. The *IR* is value of currents at − 1.00 V or − 2.00 V in the reverse regions. The *RR* values obtained at all temperatures for ***Al/GO:PTCDA/p-type S***i structures are given in Fig. 5 and Table 1. It has been seen that *RR* values decreased by increasing temperature for all temperature values. The reason for this may be that the semiconductor structure shows a good rectifier feature as charge carriers produced by photons increase due to increasing temperature. However, the values of *RR* for ± 2.00 V are slightly larger than the values obtained for ± 1.00 V. This state can be attributed to the large current values in high voltages.

Figure 6 shows variation of ideality factors versus barrier heights of the ***Al/GO:PTCDA/p-type Si*** semiconductor structure in from 80 to 420 K. According to Schmittendorf [50] and Tung [51], this state should be linear curve among ideality factor (n) and barrier height (Φ_{bo}). As seen in Fig. 6, there are two different

Table 1 The main electrical parameters *of the Al/GO:PTCDA/p-Si structures* obtained from *I-V* characteristics

T (K)	*n* *IV*	Φ_b (*eV*) *I-V*	*Saturation Currents* (I_0)	Φ_b (*eV*) *Norde*	*Rectification ratios for* ± *1.0 V*	*Rectification ratios for* ± *2.0 V*	R_S (Norde) (Ω)
80	6.398	0.221	1.894×10^{-11}	0.2431	16,316.50	20,231.42	53,842.89
100	5.106	0.278	2.431×10^{-11}	0.3046	16,175.60	20,168.80	48,696.14
120	4.222	0.337	2.685×10^{-11}	0.3693	15,280.11	19,956.88	46,640.75
140	3.541	0.392	3.969×10^{-11}	0.4297	14,145.08	19,402.99	36,217.76
160	2.992	0.452	3.906×10^{-11}	0.4961	11,836.73	18,004.37	34,673.69
180	2.591	0.511	4.016×10^{-11}	0.5645	9163.00	15,397.92	30,410.24
200	2.684	0.557	9.425×10^{-10}	0.6045	6309.19	11,191.14	25,127.77
220	2.629	0.601	2.092×10^{-10}	0.6492	5553.40	9725.16	20,290.26
240	2.437	0.646	3.991×10^{-10}	0.6967	4980.26	8251.53	12,140.93
260	2.182	0.691	7.176×10^{-10}	0.7473	4651.16	7159.09	9013.27
280	1.889	0.732	1.368×10^{-9}	0.7977	4581.94	6072.58	8228.39
300	1.790	0.765	3.208×10^{-9}	0.8300	4516.13	4989.90	6054.83
320	1.763	0.785	1.123×10^{-8}	0.8527	4010.15	4611.61	4860.18
340	1.638	0.834	1.276×10^{-8}	0.9063	4136.19	4582.04	4330.21
360	1.553	0.876	1.837×10^{-8}	0.9502	4100.92	4587.16	3228.82
380	1.470	0.918	2.475×10^{-8}	0.9965	4100.67	4589.61	2516.62
400	1.396	0.959	3.394×10^{-8}	1.0407	4108.37	4588.96	1936.45
420	1.330	0.999	4.631×10^{-8}	1.0838	4115.52	4603.60	1718.43

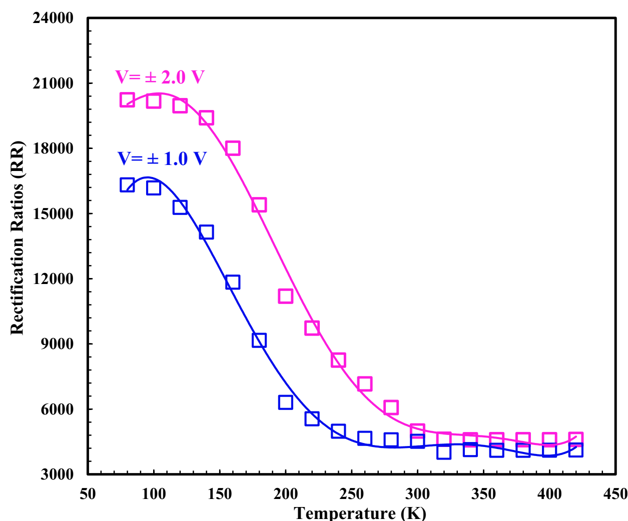

Fig. 5 Temperature-dependence rectification rates of Al/GO:PTCDA/p-Si structure at ± 1.0 V and ± 2.0 V

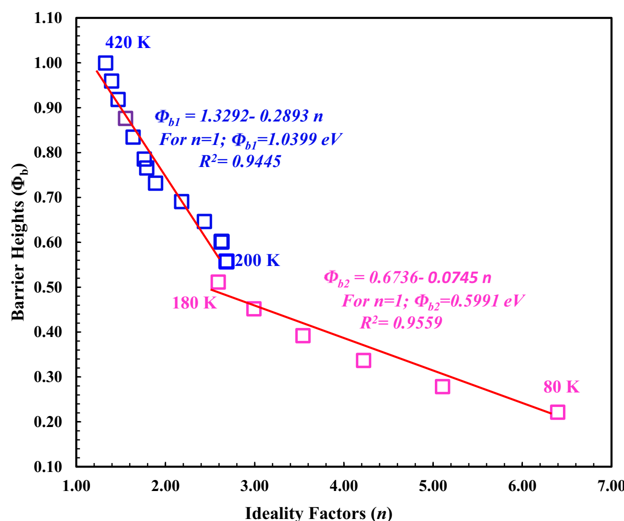

Fig. 6 Plot of barrier height vs. ideality factor for the Al/GO:PTCDA/p-Si structure

linear region that can attributed to inhomogeneities of barrier heights. The homogeneous barrier height values were determined as $\Phi_{b1} = 1.0399$ eV for the first region (200 K–420 K) and $\Phi_{b2} = 0.5991$ eV for the second region (80 K–180 K) based on extrapolation of experimental ideality factor (n) and barrier height (Φ_{bo}) curve. The Φ_{b1} value of 1.0399 eV in first region is very close the known bandgap of 1.12 eV for Si [1, 9]. However, the 0.5991 eV value in the second region is much lower than the Si bandgap. This means that for T ≤ 180 K, current transfer is controlled by the TE mechanism, and for T ≥ 200 K, it is controlled by thermionic field emission (***TFE***) mechanism [1, 9, 52, 53]. Additionally, Song et al. [54] proposed a different

model for the barrier height gaussian distribution. Essentially, this model is based on spatially inhomogeneous barrier heights at interface. Let us assume that the distribution of ***BHs*** is a Gaussian distribution with mean value $\overline{\Phi}_{bo}$ and standard deviation (σ_S). Because σ_S is generally known as a measure of barrier homogeneity [51–58]**.** Thus, the current can be expressed by the equation given below;

$$I(V) = I_0 \exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp(-\frac{qV}{kT})\right] \tag{6}$$

with

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_{ap}}{kT}\right) \tag{7}$$

here, Φ_{ap} is apparent barrier height (***BH***) and/or n_{ap} is apparent value of ideality factor. Thus, Φ_{ap} and n_{ap} are given by Refs. [1, 9, 50–54],

$$\Phi_{ap} = \overline{\Phi}_{bo} - \frac{q\sigma_o^2}{2kT} \tag{8}$$

$$\left(\frac{1}{n_{ap}} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT} \tag{9}$$

here $\boldsymbol{\rho_2}$ and $\boldsymbol{\rho_3}$ are voltage coefficient dimensionless. The apparent barrier height (Φ_{ap}) and apparent ideality factor (n_{ap}) vs. $(2kT)^{-1}$ curves are displayed in Fig. 7. As shown in Fig. 7, using Eq. 8, the intercepts and slopes of straight lines yield $\overline{\Phi}_{bo}$ and $\boldsymbol{\sigma_0}$·values of 1.3342 eV and 168.8 mV in temperature ranges 200 K–420 K (first region) and 0.7017 eV and 83.06 mV in the temperature ranges 80 K–180 K (second region) for the ***Al/GO:PTCDA/p-type Si*** semiconductor structure. This translates to two Gaussian distributions and BH in the ***Al/(GO:PTCDA)/p-type Si*** structure's rectifier region. Thus, *I–V* characteristics are affected more by inhomogeneity and potential fluctuation at low temperatures. In the same case, the graphs of $(n_{ap}^{-1} - 1)$ vs. $(2kT)^{-1}$ also showed changing properties in the two temperature ranges. Sam way, the ϱ_2 and ϱ_3 values achieved using Eq. 9 as 0.0696 eV and 0.0260 eV in the temperature ranges 200–420 K (for first region) and 0.4709 eV and 0.0055 eV from temperature ranges 80 K–180 K (for second region) for ***Al/GO:PTCDA/p-type S***i semiconductor structure. In these situation, we can say that smaller ϱ_2 and ϱ_3 voltage deformation-coefficients reveal a more extensive and widely

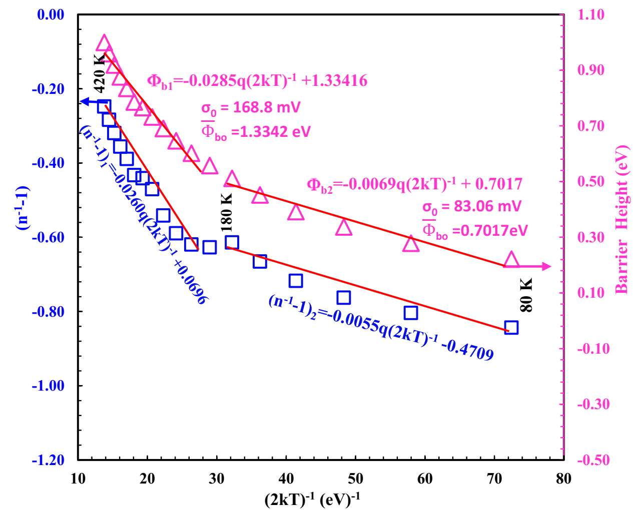

Fig. 7 Curves of Φ_{ap} (open triangles) vs. $(2kT)^{-1}$ and of $(n_{ap}^{-1} - 1)$(open squares) vs. $(2kT)^{-1}$ for a typical Al/GO:PTCDA/p-Si structure according to GDs of BHs

distributed BH in the temperature ranges 200–420 K (for first region) compared to than in the temperature ranges 80–180 K (for second region).

Furthermore, ***TFE*** and/or ***FE*** theories cannot always explain reason for larger n value at lower temperatures. Therefore, the metal-to-semiconductor barrier in homogeneity is the only way to explain the ***FE*** and ***TFE*** theories. Tung [51, 55] stated that barrier heights are inhomogeneous at low temperature. To determine Φ_{ap}, $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ and $(kT)^{-1}$ curves, actually known as Richardson curves, are given Fig. 8. Thus, Φ_{ap}, Eq. (2) can be re-written as;

$$\ln\left(\frac{I_o}{T^2}\right) = \ln\left(AA^*\right) - \frac{q\Phi_{bo}}{nkT} \tag{10}$$

The curves of $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ or $(kT)^{-1}$ are displayed in Fig. 8. In Fig. 8, it is evident that while the $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ graph appears to be linear, at low temperatures the $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ graph does not exhibit linearity. From slope of (I_o/T^2) vs. $(nkT)^{-1}$ curve, both activation energy ($E_a = \Phi_{bo}$) and A^* was calculated as 0.9005 eV and 5.4176×10^{-4} A cm^{-2} K^{-2}. In same way, from slope of $\ln(I_o/T^2)$ vs. $(kT)^{-1}$ curve, Φ_{bo} and A^* were calculated as 0.1682 eV and 3.620×10^{-9} A cm^{-2}/K^2. Nonetheless, based on the $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ plot's slope and intercept, values of activation energy and A^* were calculated to be 0.091 eV and 6.27×10^{-8} A cm^{-2} K^{-2}, respectively. From

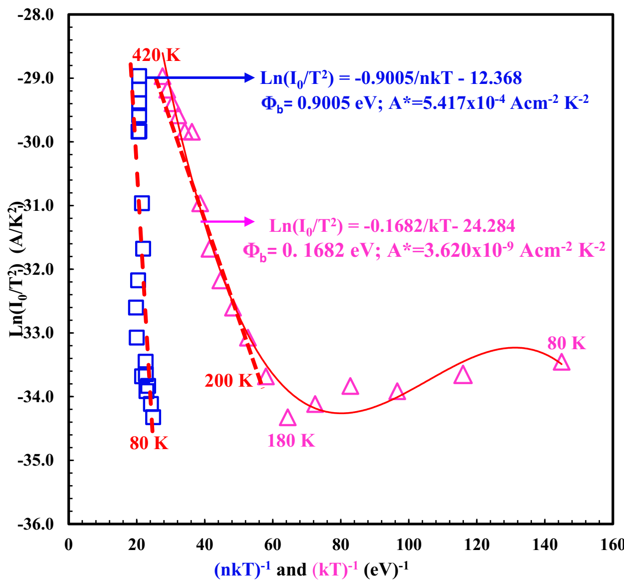

Fig. 8 Conventional activation energy ($\ln(I_0/T^2)$ vs. q/kT) plot (open triangles) and ($\ln(I_0/T^2)$ vs. q/nkT) plot (open squares) for the Al/GO:PTCDA/p-Si structure

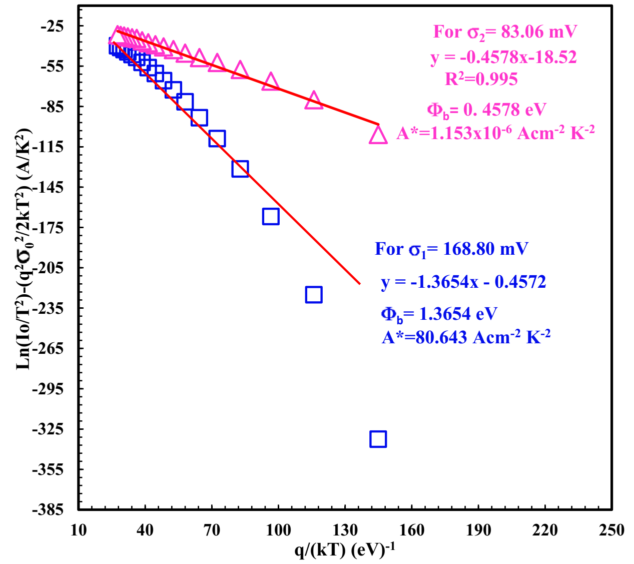

Fig. 9 Modified activation energy ($\ln(I_0/T^2)$—$q^2\sigma_o^2/2k^2T$ vs. q/kT) curves of Al/GO:PTCDA/p-Si structure according to two GDs of BHs

both $\ln(I_o/T^2)$ vs. $(nkT)^{-1}$ and $\ln(I_o/T^2)$ vs. $(kT)^{-1}$ curves, this value of A^* are substantially lower than known value of 32 A cm^{-2} K^{-2} for *p*-Si. It is evident that the A^* values for both curves are significantly less than the 32 ***Acm^{-2} K^{-2}*** known value for *p-Si* [1, 9]. This situation can be attributed to barrier height inhomogeneity and potential oscillations at interface [40, 49–55]. Horvath [59] also attributed this situation to the non-homogeneity of the barrier.

To explain these discrepancies, *GDs* of the BH, Eq. Equation (2) can be combined with Eq. (8) and rewritten as follows [37, 51];

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln\left(AA^*\right) - \frac{q\overline{\Phi}_{bo}}{kT} \tag{11}$$

Here, $\overline{\Phi}_{bo}$ is the barrier height and other abbreviations have been defined previously. The curves of $\ln(I_0/T^2)-q^2\sigma_0^2/2k^2T^2$ versus $q(kT)^{-1}$ are displayed in Fig. 9. Thus, as in Fig. 9, two distinct linear curves are present at low temperatures (among 80 K and 180 K) and high temperatures (among 200 K and 420 K). Similarly, as seen in Fig. 8, the values of $\overline{\Phi}_{bo}$ and A^* were calculated at low and high temperatures. Using Eq. 11, the values of $\overline{\Phi}_{bo}$ and A* were found to be 0.4578 eV and 1.153×10^{-6} Acm^{-2} K^{-2}in the temperature range of 200–420 K (for $\sigma_2 = 83.06$ mV). In the same way, using Eq. 11 again, the values of $\overline{\Phi}_{bo}$ and A* were found to be 1.3654 eV and 80.643 Acm^{-2} K^{-2} in the temperature range of 80–180 K (for $\sigma_1 = 168.80$ mV), respectively. Thus, especially for low temperatures (for $\sigma_1 = 168.80$ mV), the 80.643 Acm^{-2}/K^2 value of A* obtained is approximately 2.5 times larger than the known values of 32 Acm^{-2}/K^2 for *p*-Si [1, 9]. Furthermore, the series resistance (R_S) of the semiconductor structure is one of the most crucial parameters that determines electrical characteristics of any electronic device. Thus, the Φ_{bo} and R_S can be calculated using the Norde's method/theory $F(V)$, which are based on the current–voltage measurements of the semiconductor structures. Norde method [60] can be written as follows,

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{12}$$

here γ is the integer slightly bigger than n_{IV} and $I(V)$ is current values corresponding to voltage (at Fig. 3). Thus, using Eq. 12, Φ_{bo} and R_S equations can rewritten as follows;

$$\Phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{13}$$

$$R_S = \frac{\gamma - n}{I_0}\frac{kT}{q} \tag{14}$$

here, V_0 is the voltage, I_0 is the minimal current value, and $F(V_0)$ is the minimum value of $F(V)$ that corresponds to the lowest point of $F(V)$. Figure 10 shows

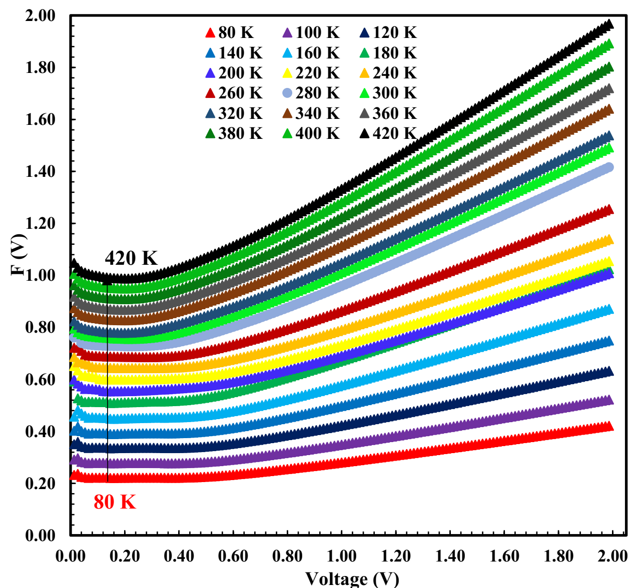

Fig. 10 F(V)–V plots of Al/GO:PTCDA/p-Si structure changing temperature from 80 to 420 K

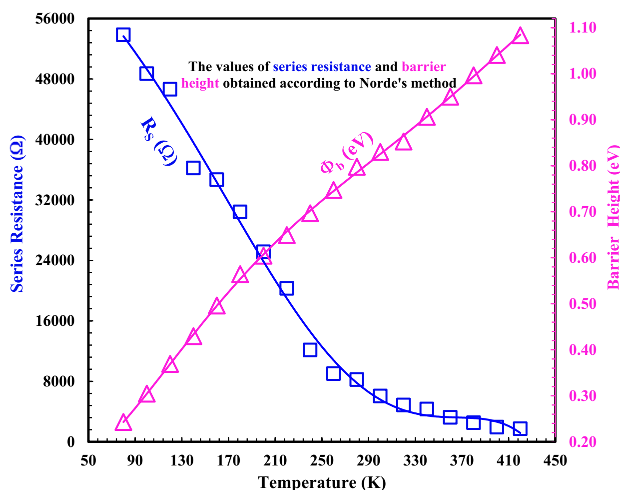

Fig. 11 Variation of barrier height and series resistance obtained from the Norde function for the Al/GO:PTCDA/p-Si structure as a function of temperature

the *F(V)-V* curves of the Al/(GO:PTCDA)/*p*-Si semiconductor structure in temperature ranges from 80 to 420 K. Thus, using Eq. 11 and Eq. 12, the R_S and Φ_b values obtained from Norde functions for the ***Al/GO:PTCDA/p-Si*** semiconductor structure in the temperatures among 80 K and 420 K are given in Table 1 and Fig. 11. Furthermore, Φ_b values calculated from the Norde functions are also included in Fig. 4. Thus, the Φ_b and R_S values obtained from the $F(V) - V$ plots were 0.2431 eV and 53.842 kΩ at 80 K and 1.0838 eV and 1.718 kΩ at 420 K. As seen in Fig. 11 and Table 1, while Φ_b values increased with increasing temperature, R_S values decreased. The increase in carriers in the semiconductor structure is the cause of this drop in series resistance with temperature. That is, it is evident that the Φ_b values derived from the Norden technique are marginally greater than those derived from the *TE* theory. Basically, this can be attributed to the fact that the Norde theory is applied to all forward bias *lnI-V* graphs, whereas it is solely applied to linear region (low voltages) from TE theory.

4 Conclusions

The surface morphologies of ***GO*** and ***PTCDA*** thin films were investigated using UV/Vis and SEM analyses. The electrical properties of the ***Al/GO:PTCDA/p-type S***i structure were examined in the temperature ranges from 80 to 420 K with 20 K intervals. Electrical parameters such as n, Φ_{bo}, I_0, RR, and R_S were obtained separately from *I-V* measurements for each temperature value (including room temperature). The ***GD*** gives mean $\overline{\Phi}_{bo}$ of 1.3342 eV and 0.7017 eV and standard deviations (σ_o) of 168.8 mV and 83.06 mV. Furthermore, the values of $\overline{\Phi}_{bo}$ and A^* were calculated from a revised $\ln(I_0/T^2) - q^2 \sigma_o^2 / 2k^2T^2$ vs. q/kT plot as 0.4578 eV and 1.153 × 10^{-6} A cm^{-2} K^{-2} (for σ_2 = 83.06 mV) and 1.3654 and 80.643 × 10^{-6} A cm^{-2}/K^2 (for σ_1 = 168.80 mV), respectively. The 80.643 Acm^{-2}/K^2 value of A* obtained is larger than the known value of 32 Acm^{-2}/K^2 for ***p-type Si***. This means that ***Al/GO:PTCDA/p-type S***i semiconductor structures correspond to two different GDs and BHs in the rectifier area. In conclusion, the *I–V-T* properties of ***Al/GO:PTCDA/p-type S***i semiconductor structures have been easily explained in terms of the *TE* mechanism by ***BHs*** of the ***GD***, and hence such a structure can be tailored for temperature-dependently actuated ***GO*** and ***PTCDA***-based electronic devices.

Author contributions

All of the authors contributed to the conception of this research, the practical experimentation, the analysis of the results, and the writing of the manuscript.

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Data availability

All data and materials are available from the corresponding author upon reasonable request.

Material availability

All data and materials are available from the corresponding author upon reasonable request.

Declarations

Conflict of interest The authors declare that there is no conflict of interest.

Consent to participate All the authors declare their consent to participate in this research article.

Consent for publication All the authors declare their consent for publication of the article on acceptance.

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